Quaternary digital to analog signal converters

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Possibilities and principles for design of quaternary digital to analog signal CMOS converters are proposed and described in the paper. Such converters perform signal conversion from quaternary digital signals into analog signal and can be used in CMOS quaternary digital systems. General structure and principle for design of CMOS quaternary to analog converters are proposed and described first. Then, some concrete circuits for implementation of two digit CMOS quaternary digital to analog signal converters are proposed as an illustration of the design. Two types of the converters are described: powerful type converters and simple type converters. All given solutions have been analyzed and all descriptions and considerations have been confirmed by computer simulations.

1 Introduction

Practically used digital systems are dominantly binary ones. Reasons and possibilities for application and implementation of digital systems that use logic basis greater than 2 (so called multiple-valued or MV systems and logic) are becoming real and practically feasible with rapid development of VLSI technologies [1-5]. The greatest practical interest exists for research and implementation of ternary (logic basis 3) and quaternary (logic basis 4) MV circuits and systems [1-5].

There are many very known advantages of quaternary logic systems and circuits comparing with the binary ones: greater speed of logic and arithmetic operations, greater density of memorized information, better usage of transmission lines and paths, decreasing of interconnections complexity and area, decreasing of pin number of integrated circuits and printed boards, possibilities for easier testing of digital systems [1-5].

The reasons and advantages of application of CMOS technology in binary digital circuits and systems are very well known. All these good characteristics should be also kept in MV logic circuits and systems. There are also some advantages of CMOS technology that arecharacteristic for MV logic [1-5]. Also, since first descriptions of MV logic the greatest interest exists for implementation in CMOS technology.

Possibilities and principles for design and implementation of quaternary digital signals to analog signal converters for application in quaternary CMOS digital systems are proposed in the paper. First, general structure and principle for converters design and implementation are considered and described. Then, as an illustration example of converters design, the concrete circuits for two digit CMOS quaternary to analog signal converters are proposed. Two types of the converters are described: so called powerful type converters and so called simple type converters. All proposed principles and solutions were analyzed and confirmed by PSpice computer simulations.

2 Quaternary digital to analog signal converter structure

General circuit structure and principle for design and implementation of quaternary CMOS digital to analog converter are proposed and shown in Fig.1. There are more (n) quaternary digital input signals (D_i) and one analog output signal (A_O and V_O).

Shown and proposed structure in Fig.1 uses CMOS parallel voltage comparator network at the inputs, CMOS binary encoder network and CMOS output network. The comparator network and binary encoder network are supplied by two supply voltages corresponding to two binary states: V_{SS} (binary logic 0) and V_{DD3} (binary logic 1). The quaternary logic levels are V_{SS} (quaternary logic 0), V_{DD1} (quaternary logic 1), V_{DD2} (quaternary logic 2) and V_{DD3} (quaternary logic 3). The output network is supplied by more supply voltages ($m=4^n$) corresponding to all possible (m) levels of output analog signal (V_{DDOi}).

The input comparator network performs comparison of input quaternary signals (D_i) with appropriate threshold voltages and performs conversion of quaternary signals into binary ones (B_i). Since here is conversion from quaternary to binary signals, there are existing three threshold voltages. The threshold voltages are in the middle between voltage levels of quaternary digital signal. This network in principle can be implemented in the same way as standard binary CMOS voltage comparator network. For realization can be used standard CMOS binary voltage comparator circuits. This network gives binary output signals (B_i) with voltage levels of V_{SS} and V_{DD3}.

The binary encoder network performs encoding of comparator network output signals (B_i) into appropriate binary signals (C_i) for control of output network. This network can be realized in the same way as standard binary CMOS encoder network. For realization can be

used standard CMOS binary logic circuits. It gives binary output signals (C_i) with voltage levels of V_{SS} and V_{DD3}.

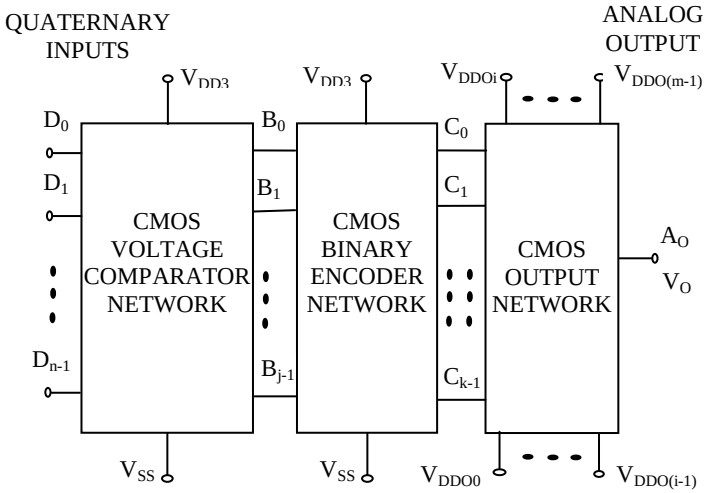

Figure 1. Structure of CMOS quaternary digital to analog signal converter.

The output network generates needed output analog signal (A_O) and analog output voltage (V_O) according to states at outputs of binary encoder logic network (C_i). Since here is quaternary to analog signal converter, there are existing $m=4^n$ possible output voltage levels, where n is number of quaternary digital inputs. Number of output voltage levels depends on converter resolution, i.e. on number of quaternary digital inputs. Needed output voltage levels are obtained using appropriate $m=4^n$ supply voltages (V_{DDOi}) in the range from V_{SS} to V_{DD3}.

It should be performed separately design and implementation of CMOS voltage comparator network, CMOS binary encoder network and CMOS output logic network in the proposed circuit structure in Fig.1. The complexity of design of all three networks depends on number of quaternary inputs n and increases with increasing of n. Design of such converters includes determination of number of quaternary inputs, selection of used output network, selection of used voltage comparators and design of appropriate encoder network.

The structure proposed in Fig.1 is general one. It gives possibility to develop and design CMOS quaternary to analog converter with any number of quaternary inputs and with any resolution. As an illustration of development and design of such converters, here will be shown way for design of two digit CMOS quaternary to analog converters.

3 Two digit quaternary digital to analog signal converter

Two types of CMOS quaternary to analog converters with two quaternary inputs will be proposed and described: powerful type converters and simple type converters. Based on the proposed structure it can be realized more different concrete solutions of the converters. It will be proposed solutions that are the most appropriate for some applications. First will be shown solutions of so called powerful type converters that have higher output power and use more MOS transistors. Then will be proposed so called simple type converters that have smaller number of transistors and lower output power.

3.1 Powerful type converters

Proposed basic circuit of powerful type two digit CMOS quaternary to analog converter is shown in Fig.2. The circuit has one analog output (A_O) and two quaternary inputs (D_0 and D_1). It uses simple CMOS output network. The CMOS voltage comparator network consists of six (three for each quaternary input) voltage comparators (VC_i). Each comparator has three appropriate threshold voltages ($V_{R0,}$ V_{R1} and V_{R2}) for comparison with input quaternary signal. The threshold voltages should be equal to the voltages that are in the middle between neighboring quaternary voltage levels. Each comparator compares the input quaternary signal with its threshold voltage and gives appropriate binary output signal (B_i). For implementation of this comparator network can be used standard CMOS voltage comparator circuits.

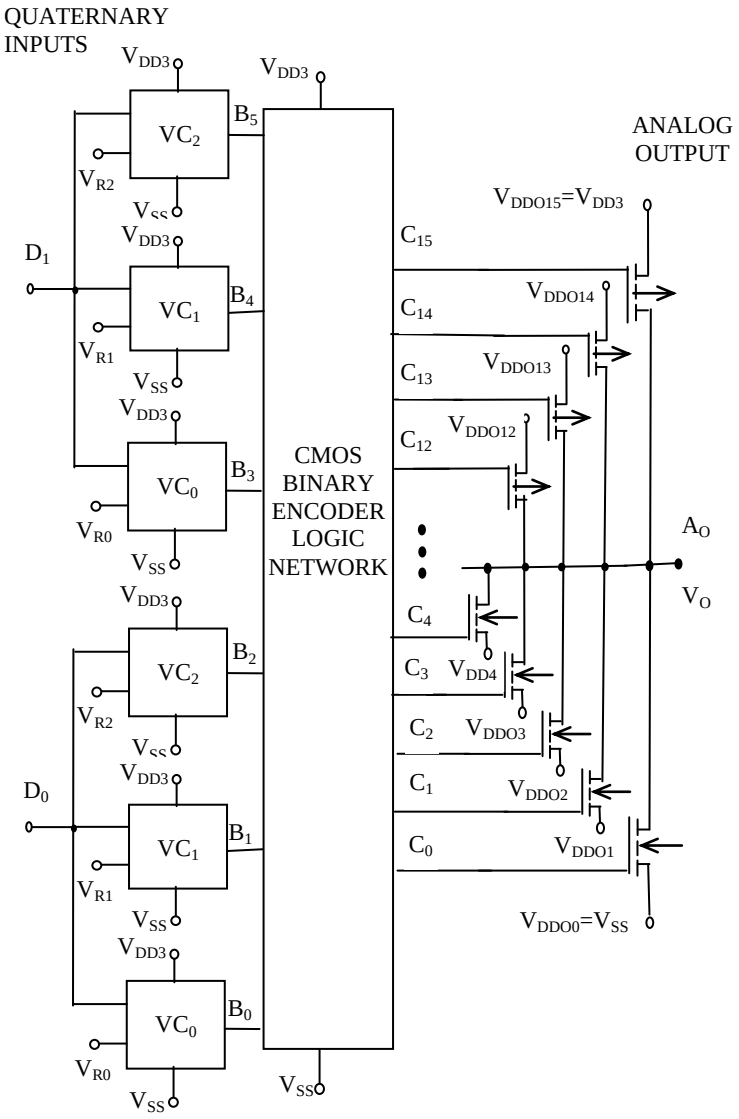

Figure 2. Two digit powerful type quaternary digital to analog signal converter.

The CMOS encoder network encodes the comparator network output signals (B_i) into appropriate binary signals (C_i) for control of output network. There are six encoder network input signals (B_i) here and sixteen output signals (C_i). This network can be realized in the same way as appropriate binary CMOS encoder network. Standard CMOS binary logic circuits can be used for implementation of the encoder network.

The CMOS output network generates needed output analog signal (A_O) and output voltage (V_O) according to states at outputs of binary encoder logic network (C_i). It is proposed appropriate output network here. The proposed output network uses only MOS transistors and is the simplest one with the greatest output power. It is shown the principle of design and one part of the output network in Fig. 2.

The way of operation of the two digit quaternary to analog converter from Fig.2 can be shown using logic table. Based on the logic table it can be designed appropriate CMOS binary encoder network. It can be obtained appropriate logic expressions for encoder logic outputs (C_i) as a function of encoder logic inputs (B_i). Based on obtained expressions it can be designed appropriate encoder logic circuits. Standard binary CMOS inverting logic circuits (inverters, NAND and NOR logic circuits) can be used for design of the encoder network. Such can be obtained CMOS quaternary to analog signal converter of powerful type with minimized number of used transistors.

3.2 Simple type converters

Design of quaternary to analog CMOS converters with smaller total number of transistors can be obtained if it is used different implementation of binary encoder network and different output network compared with the powerful type converters. Depending on the design of encoder network and output network it can be obtained more different designs of complete quaternary to analog converter.

Proposed output network of simple type two digit CMOS quaternary to analog converter with minimal number of MOS transistors is shown in Fig.3. This simple type converter has also two quaternary inputs (D_0 and D_1) and one analog output (A_O). It uses modified CMOS output network designed using serial and parallel connections of MOS transistors. This way of design enables to avoid usage of specially designed encoder CMOS network and to use only output signals of voltage comparators for direct control of transistors in the output network. This design drastically reduces total number of used MOS transistors comparing with the powerful type quaternary to analog converter. But, serial connections of MOS transistors in output network increase propagation delay time and conversion time of the simple type converter compared with the powerful type one. It also creates different output powers and different delay times for different output voltage levels comparing with the powerful type converter what is also a disadvantage of the simple type converters. Table I also shows the way of operation of simple type two digit quaternary to analog converter.

It is shown the principle of such design and one part of the output network in Fig. 3.

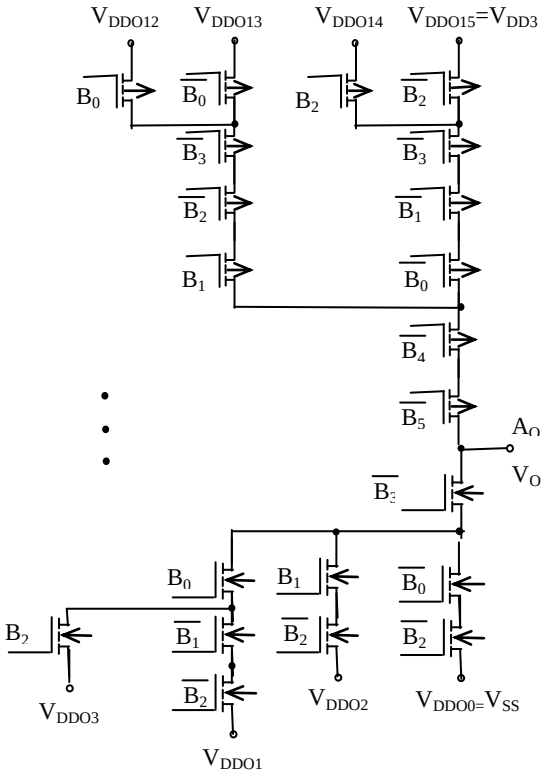

Figure 3. Output network of simple type two digit quaternary to analog converter.

3.3 Simulation results

Operations of proposed powerful type and simple type converters were analyzed by PSpice simulations. Technology parameters of one CMOS process [5] and supply voltages V_{SS}= 0V, V_{DD1}=10V, V_{DD2}=20V and V_{DD3}=30V were used in simulations. Voltage CMOS comparator circuits as proposed in the paper [6], with appropriate designed threshold voltages, are used for design of voltage comparator network of analyzed quaternary to analog converters. The voltage comparator circuits are based on the circuits proposed and described in the paper [7]. Timing diagrams of output voltage as a function of input quaternary voltages for two digit powerful type converter obtained by PSpice simulations are shown in Fig.4. At quaternary inputs were applied signals for obtaining of all possible output voltage levels. Such is confirmed correct operation of the circuit and proper conversion of quaternary signals into analog signal. By the simulation was confirmed that the same signal forms are valid also for the simple type two digit quaternary to binary converter.

The simulations confirm that powerful type converters have smaller conversion times compared with simple type ones for applications with greater capacitive loads. In applications with smaller loads the simple type circuits have better this characteristic. Fig.5 shows conversion times (t_c) of two digit powerful type and simple type quaternary to analog converter as a function of capacitive

load C_L obtained by PSpice simulations. In simulations were used the same technology parameters and the same supply voltages as in previous simulations. By full line are shown results for powerful type converter and by dashed line are shown results for simple type converter.

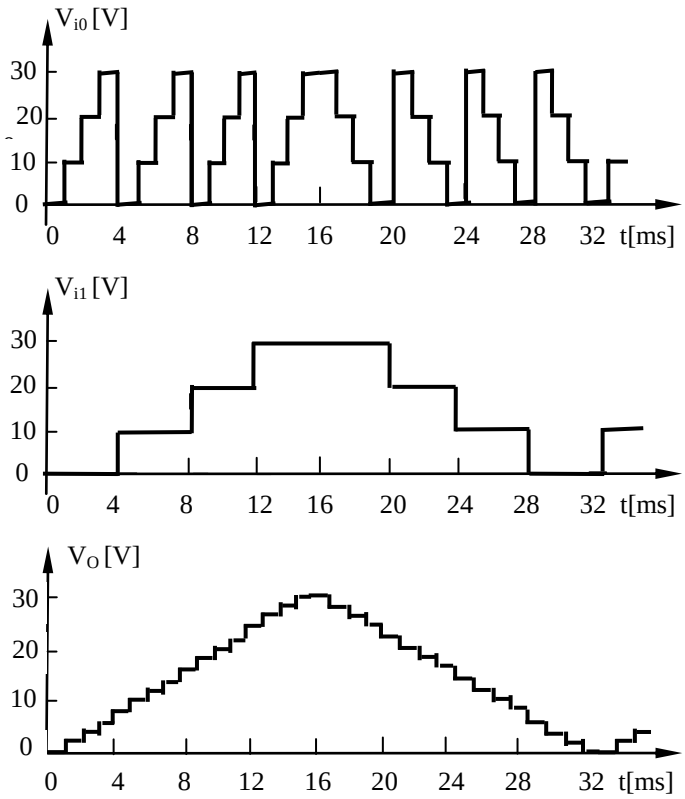

Figure 4. Timing diagrams for powerful type quaternary to analog converter.

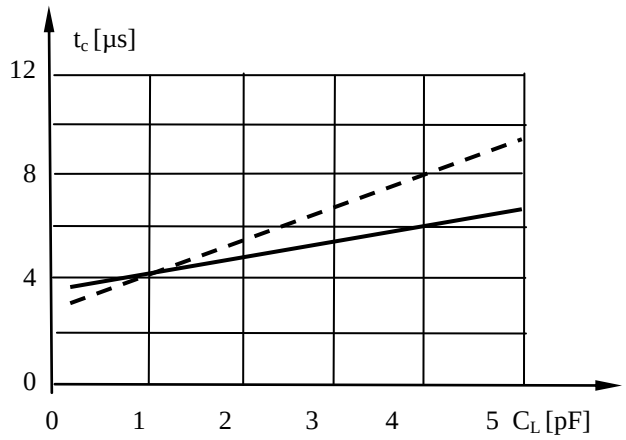

Figure 5. Conversion times of two digit quaternary to analog converters as a function of capacitive load.

4 Conclusions

Well known advantages of MV digital systems are the main reasons for increase of interest for application of such digital systems. Practically the greatest interest exists for quaternary CMOS MV systems. As well as in the binary digital systems there is needed for digital to analog conversion and such converters in MV digital systems.

Proposed principles for design of CMOS quaternary to analog converters are clear and relatively simple. For implementation are used only standard MOS transistors and standard MOS technology. Proposed principles enable design of converters with any (needed) number of quaternary logic inputs and with any (needed) resolution, according to needed working conditions. Obtained converters are fully CMOS ones without static power consumption if we neglect leakage currents.

Described principles and solutions enable to obtain optimal converter depending on requirements of application. The simple type converters are simpler and use smaller total number of transistors but have greater conversion times for greater loads. The powerful type converters are more complex and use more transistors but have smaller conversion times for greater loads. The simple type converters should be used in applications with smaller loads and smaller needed working speeds. The powerful type converters should be used in applications with greater loads and greater needed working speeds.

Parameters of one older CMOS technology process have been used in simulations in order to be possible to compare results of the simulations with earlier obtained results for some other circuits.

References

[1] E. V. Dubrova, "Multiple-valued logic in VLSI: challenges and opportunities", Proceedings of Conference NORCHIP'99, 1999, pp. 340-350.

[2] E. V. Dubrova, "Multiple -Valued Logic in VLSI Design", International Journal on Multiple -Valued Logic, 2002.

[3] V. Patel, K. S. Gurumurthy, "Quaternary CMOS Combinational Logic Circuits", Proceedings of International Conference on Information and Multimedia Technology, 2009., pp.538-542.

[4] V. Patel, K. S. Gurumurthy, "Quaternary Sequential Circuits", International Journal of Computer Science and Network Security, July 2010., pp. 110-117.

[5] C. H. Diaz et all., "An accurate analytical delay model for BiCMOS driver circuits", IEEE Transaction on Computer-Aided Design, no. 5, 1991., pp. 577-588.

[6] D. Bundalo, Z. Bundalo, F. Softić, M. Kostadinović, "Interconnection of quaternary and binary CMOS digital circuits and systems", Proceedings of International Scientific Conference ERK2011, Portorož, Slovenia, September 2011., pp.51-54.

[7] Z. Bundalo, "CMOS and BiCMOS logic circuits for conversion from low to high logic level", Proceedings of the 51st Conference ETRAN, Herceg Novi -Igalo, Montenegro, June 2007., pp. EL2.1-1-4 (in Serbian).