A CMOS BANDGAP VOLTAGE REFERENCE DESIGN

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Abstract. *This paper details design process of a bandgap voltage reference circuit in a 350 nm CMOS technology process. Purpose of the bandgap reference circuit is to provide temperature, process and power supply independent reference voltage. Throughout the paper, design considerations to achieve better stability of the output voltage are presented. The design underwent several Monte-Carlo and corner simulations. Simulations have produced results showing a bandgap voltage of* 1.208 ± 0.009 *V (3* σ*), TC of* 9.330 ± 4.026 *ppm/K (*σ*) and DC PSRR of* -67.707 ± 0.981 *dB (3* σ*).*

1 Introduction

A Bandgap voltage reference circuit is an important part of many analog and mixed electronics systems, such as analog-to-digital converters (ADCs), digital-to-analog converters (DACs), voltage regulators, flash memories ... Its primary function within these systems is to deliver better accuracy and stability due to its ability to maintain constant voltage, regardless of variations in temperature, process and supply voltage. Generated voltage is roughly equivalent to the intrinsic bandgap voltage of the used semiconductor. Silicon produces output voltage of around 1.205 V.

An output bandgap voltage is obtained with a sum of proportional to absolute temperature (PTAT) and complementary to absolute temperature (CTAT) voltages. A CTAT voltage is generated using a forward biased p-n junction, such as a diode or a diode-connected BJT, while a PTAT voltage is acquired by a difference of two base-emitter voltages. PTAT voltage dependence of ΔU_{BE} derives from the thermal voltage (U_T). Due to the higher temperature coefficient (TC) of CTAT ($TC \approx -2$ mV/K), the PTAT ($TC \approx 0.085$ mV/K) voltage must be multiplied by a scaling factor of K. Figure 1 demonstrates generation of bandgap voltage via block diagram.

The designed bandgap circuit is based around commonly used topology, proposed by H. Banba [1]. Circuit has been designed as a part of a 350 nm CMOS integrated inductive encoder, similar to the one described in [2].

2 Banba's bandgap voltage reference

As previously mentioned, the core of the designed circuit utilizes Banba's bandgap voltage reference. Therefore, this section will be devoted to a brief presentation of this topology. The circuit diagram of the discussed topology is shown in Figure 2. In order to generate bandgap voltage, firstly PTAT and CTAT components must be extracted. As discussed in Section 1, CTAT voltage is generated using diode-connected BJT Q_1, whereas PTAT voltage is established by the voltage difference between Q_1 and Q_2. The discussed topology initially turns PTAT and CTAT components into currents via resistors R_1 and R_2 and adds them up. If the scaling factor K is chosen in such a manner that the influences of PTAT and CTAT components cancel out, resulting current is temperature independent. Assuming all PMOS transistors have the same dimensions, current flowing through a resistor R_4 is mirrored from Q_3, and can be expressed with the [3, eq. (1)]. The expression in parentheses reveals the bandgap voltage generation components, displayed in Figure 1, where the term $R_2 \ln n / R_1$ represents the scaling factor K, with n denoting the difference in current densities of transistors Q_2 and Q_1.

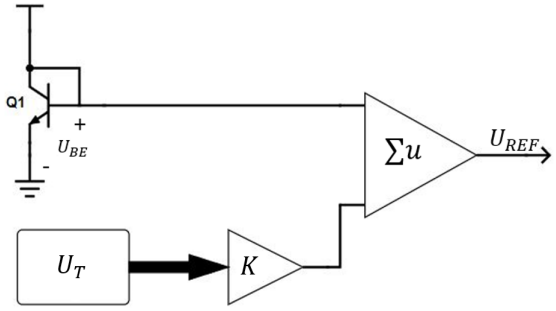

Figure 1: Block diagram of a bandgap voltage generation

$$|I_{D3}| = |I_{R4}| = (U_{EB1} + R_2(U_T \ln n)/R_1)/R_2 \quad (1)$$

Temperature-independent current I_{R4} flowing through resistor R_4 generates bandgap voltage, as shown in [3, eq. (2)].

$$U_{REF} = R_4(U_{EB1} + R_2(U_T \ln n)/R_1)/R_2 \quad (2)$$

The value of the K-factor can be calculated using (3).

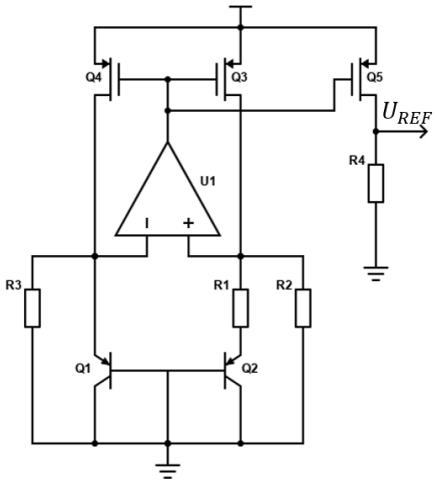

Figure 2: Banba's bandgap voltage reference

$$K = R_2 \ln n / R_1 = |TC_{CTAT}| / TC_{PTAT} \qquad (3)$$

3 Circuit design

The proposed circuit, shown in Figure 4, is composed of two parts, namely the bandgap voltage reference circuit and the start-up circuit. The start-up circuit was added due to the bandgap circuit constraint, often referred to as the "start-up problem", that has the potential to drive the circuit into a "degenerate" operating point during the power-up.

3.1 Bandgap voltage reference circuit

Because the chosen topology was already described in Section 2, this subsection will only cover some of the design problems and additional features of the designed circuit.

Starting the design, appropriate operational amplifier topology needed to be chosen. To obtain high DC gain, high unity bandwidth and low susceptibility to power supply variations, folded cascode amplifier was designed, as shown in Figure 3.

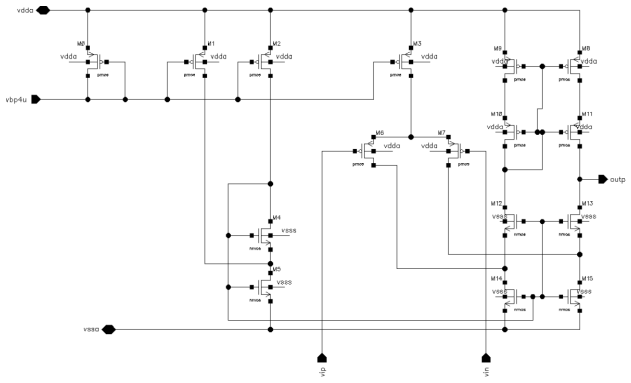

Figure 3: Folded cascode amplifier

Moving on to the top design of the bandgap circuit, previously discussed idealized model does not consider temperature dependencies of resistors. Consequently, the current flowing through the branches of the bandgap core will now feature an additional temperature-dependent component, which will be compensated for by the output resistor, if their temperature coefficients are inversely proportional.

Some adjustments were made to improve circuit's Power Supply Rejection Ratio (PSRR). To increase low-frequency PSRR, PMOS current mirrors were cascoded and their lengths were made relatively high. Meanwhile, to increase high-frequency PSRR, an output decoupling capacitor was added.

To increase the functionality of the proposed circuit, an output buffer was added. The output buffer increases driving capabilities of the circuit and prevents the core of the bandgap voltage to be effected by an external load.

3.2 Start-up circuit

As it has been already mentioned, the start-up circuit was added to prevent the bandgap circuit from operating in the wrong operating point. In Figure 4, it is situated on the left side of the circuit and it is composed of a non-inverting Schmitt trigger and MOSFETs M_9, M_{10}, M_{11}, M_{12} and M_{13}.

Let's assume that the start-up circuit is not present and an incorrect operating point is established. In this scenario, no current is flowing through the branches of the structure, leading to the potential of *vbe1* and *vbe10* being zero. To "push" the bandgap circuit out of the "degenerate" point, current should be supplied to operational amplifier's negative terminal. The supplied current, causes positive feedback loop, given that the amplifier's gain is negative, so is the gain of the common-source PMOS transistors. The current flowing through the branches is continuously rising till it obtains the second stable operating point.

Moving on to the designed start-up circuit, supply voltage ramp-up causes current increase through PMOS M_{12}. NMOS transistors M_9, M_{10} and M_{11}, width to length ratios are set in such a way that they present high resistance relatively to M_{12}. In that way, most of the voltage resides on them. If the voltage is below the upper hysteresis threshold value of the Schmitt trigger, PMOS M_{13} will be turned on and it will supply the bandgap circuit with additional current. Once the voltage exceeds the upper threshold, M_{13} will be turned off and circuit will be able to operate by itself in the correct operating point.

4 Simulation results

4.1 DC analysis

In order to analyze behavior of the output with respect to changes in temperature, a DC temperature sweep analysis was performed over a broad temperature range of -40 °C to 125 °C. Figure 5 illustrates output voltage curves for different process corners. To determine temperature coefficients from the provided curves, the box method [4] was used. Calculated results are gathered in Table 1. As

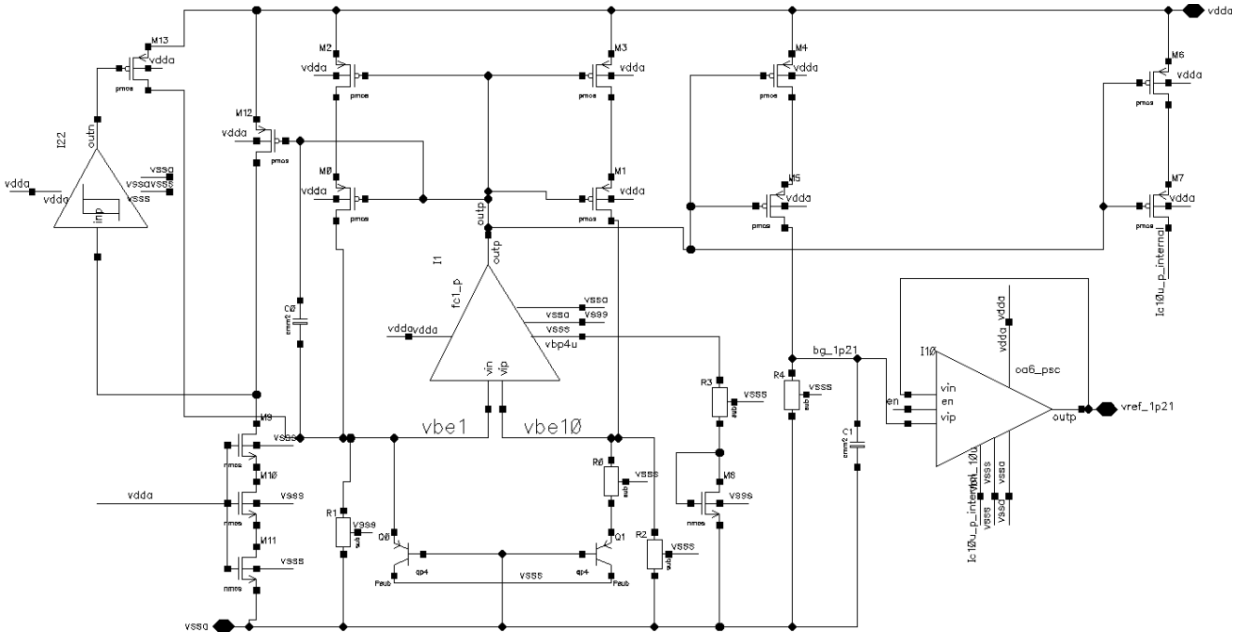

Figure 4: Circuit diagram

it can be seen, the designed circuit produces satisfactorily stable results, with the worst TC of 11.170 ppm/K.

Table 1: Temperature coefficient for various process corners

Corner	tm	wo	wp	ws	wz
TC [ppm/K]	5.792	5.512	11.170	9.802	6.188

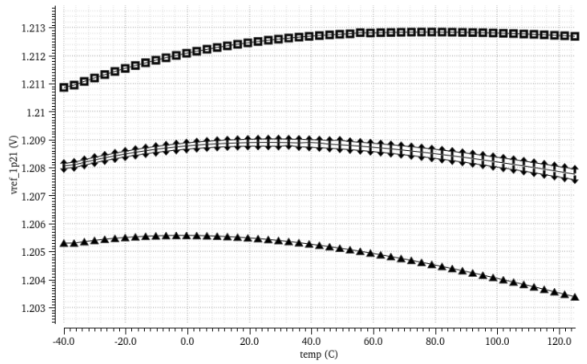

Figure 5: DC corner simulation of the bandgap voltage
□: ws ↓: wz ▲: wp
—: tm ↑: wo

4.2 Transient analysis

To analyze the start-up and validate circuit's stability, transient analysis was performed. To cover a range of possible scenarios, different supply voltage ramp-up slopes (ranging from few V/ns to few V/ms) were used and all the simulations ran across different process corners and temperatures (-40°C, 27°C, 125°C). Figure 6 illustrates the results of the 0.5 V/us supply voltage ramp-up. As it can be seen, output voltage successfully stabilizes, with the worst settling time of 3.702 us.

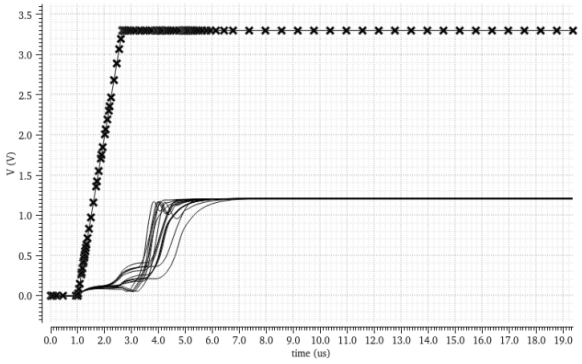

Figure 6: Transient simulation of the start-up
—: Output voltage ×: Supply voltage

4.3 AC analysis

In order to analyze behavior of the output with respect to changes in supply voltage, an AC analysis was performed. An AC voltage source, whose frequency was swept across 10 MHz region, was superimposed to the DC power supply. For every frequency point, PSRR was measured, as it can be seen in Figure 7. Worst AC PSRR, with a value of -10.072 dB, was obtained at 1.315 MHz. Typical DC PSRR value is -67.703 dB and the worst one is -66.166 dB.

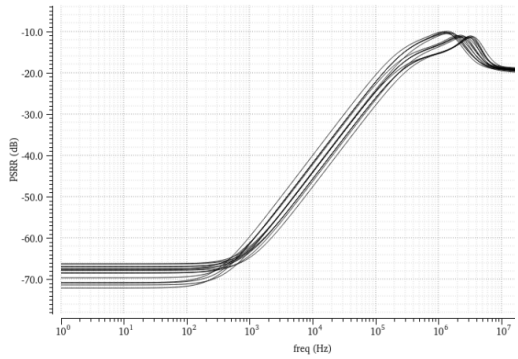

Figure 7: PSRR simulation

4.4 Monte-Carlo simulations

To further analyze the designed circuit, Monte-Carlo simulations were performed. Simulations used 3-σ Gaussian distribution and they were executed at 1000 different points. Figure 8 illustrates results of Monte-Carlo simulations of the bandgap voltage. Mean value of the obtained points is 1.208 V with 3 σ margin of 9 mV.

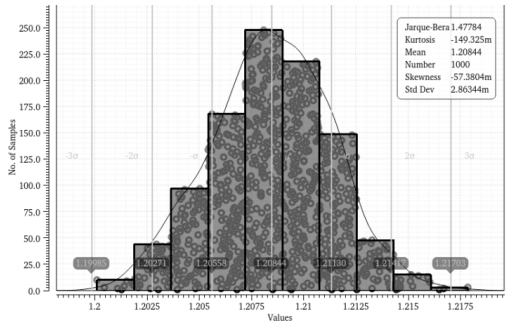

Figure 8: MC simulation - bandgap voltage

Results of temperature coefficient Monte-Carlo simulations are shown in Figure 9. The obtained histogram exhibits asymmetrical distribution with mean value of 9.330 ppm/K and standard deviation of 4.026 ppm/K.

Lastly results of DC PSRR Monte-Carlo simulations are shown in Figure 10. Mean value of the obtained points is -67.707 dB, with 3 σ margin value of 981 mdB.

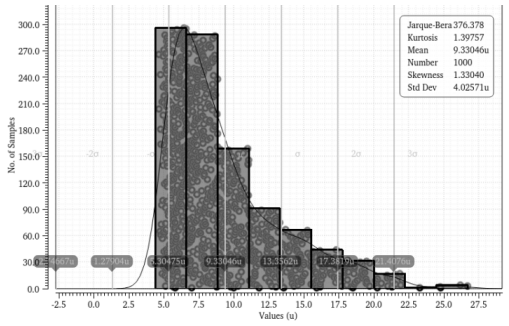

Figure 9: MC simulation - TC

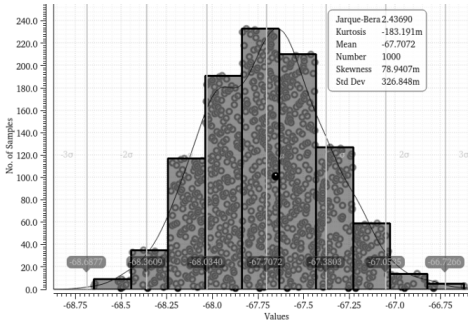

Figure 10: MC simulation - DC PSRR

5 Conclusion

A CMOS bandgap voltage reference has been successfully designed and simulated. Corner simulations revealed the worst TC of 11.170 ppm/K, worst DC PSRR of -66.166 dB and the longest settling time of 3.702 us. Further analysis of the circuit, using MC simulations, revealed that the device mismatch introduces additional error to some of the previously simulated results. MC simulations have produced results showing a bandgap voltage of 1.208 ± 0.009 V (3 σ), TC of 9.330 ± 4.026 ppm/K (σ) and DC PSRR of -67.707 ± 0.981 dB (3 σ).

Circuit could further be improved with additional circuitry, to minimize process variations of the bandgap voltage.

6 Acknowledgment

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